

What is claimed is:

1. A method for setting a clock, applied in a clock generating device of a computer motherboard and setting the clock according to a signal status of a basic input/output system (BIOS), the method comprising:
 - 5 detecting if a signal output from the BIOS is irregular;
 - replacing an original setting value of a memory inside a logic control unit by a frequency setting value pre-stored in a memory unit if the signal output from the BIOS is irregular; and
 - finishing an auto-booting process.
- 10 2. A method for setting a clock, applied in a clock generating device of a computer motherboard and setting the clock according to a trigger signal, the method comprising:
 - detecting if the trigger signal is input;
 - replacing an original setting value of a memory inside a logic
 - 15 control unit by a frequency setting value pre-stored in a memory unit if the trigger signal is input; and
 - finishing an auto-booting process.
3. The method as claimed in the claim 2, wherein the trigger signal is a high-voltage trigger signal or a low-voltage trigger signal.
- 20 4. A device for setting a clock, which is a clock generating device of a computer motherboard, comprising:
 - a crystal oscillator;
 - a frequency control unit;
 - a phase-lock-loop (PLL) spread-spectrum unit electrically

connected with the crystal oscillator and the frequency control unit;
a memory unit having a clock setting value stored therein;
a detection control unit electrically connected with the memory unit
and used to detect a signal status; and

5 a logic control unit electrically connected with the PLL
spread-spectrum unit, the frequency control unit and the detection
control unit.

5. The device as claimed in the claim 4, wherein the memory unit is an
electrically erasable programmable read-only memory (EEROM), an
10 erasable programmable read-only memory (EROM) or a flash memory.

6. The device as claimed in the claim 4, wherein the signal status detected
by the detection control unit is an output signal status of a BIOS.

7. The device as claimed in the claim 4, wherein the signal status detected
by the detection control unit is a trigger signal status.

15 8. The device as claimed in the claim 4, wherein the clock setting value
stored in the memory unit is an operating clock value of the logic
control unit stored in the memory unit by the detection control unit
when the detection control unit detects a BIOS as working regularly.

9. The device as claimed in the claim 6, wherein the clock setting value
20 stored in the memory unit is an operating clock value of the logic
control unit stored in the memory unit by the detection control unit
when the detection control unit detects a BIOS as working regularly.

10. The device as claimed in the claim 4, wherein the clock setting value
stored in the memory unit is set by a BIOS.

11. The device as claimed in the claim 4, wherein the clock setting value stored in the memory unit is a fixed value.